JOINT INSTITUTE FOR NUCLEAR RESEARCH
Dzhelepov Laboratory of Nuclear Problems

FINAL REPORT ON THE START PROGRAMME

Optical link integration and validation between L2 and L1 concentrators for the SPD experiment

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Contents

Abstract

This paper describes the integration of the connection and the stability and quality checks for this connection between L1 and L2 concentrators. These concentrators function as the data transport lines in the readout chain of the SPD experiment.

We demonstrate the testing of this optical link to verify the stability of the Ethernet modules responsible for data transmission between the L1 and L2 boards. This verification is crucial for ensuring reliable data acquisition.

Furthermore, the paper describes a module designed to decapsulate Raw Ethernet packets containing slow control commands received from L2.

1 Introduction

This paper details the integration and testing of the connection between L1 and L2 concentrators within the readout chain of data acquisition (DAQ) system for the Spin Physics Detector (SPD) experiment at the Nuclotron-based Ion Collider fAcility (NICA). The SPD aims to conduct experiments in spin physics, explore the limits of nuclear matter existence, and achieve a comprehensive understanding of proton structure. During experiments, the detectors will record particle characteristics, generating a data stream with an estimated rate of approximately 20 GB/s. This stream includes both physics data and commands for controlling the DAQ system [1].

To manage this high bandwidth, the DAQ system requires specialized electronics capable of receiving and performing multi-level processing on the data stream, while maintaining maximum throughput and aggregating data streams into a DAQ server. Software then performs event building and data processing. The DAQ readout architecture is illustrated in Figure 1.

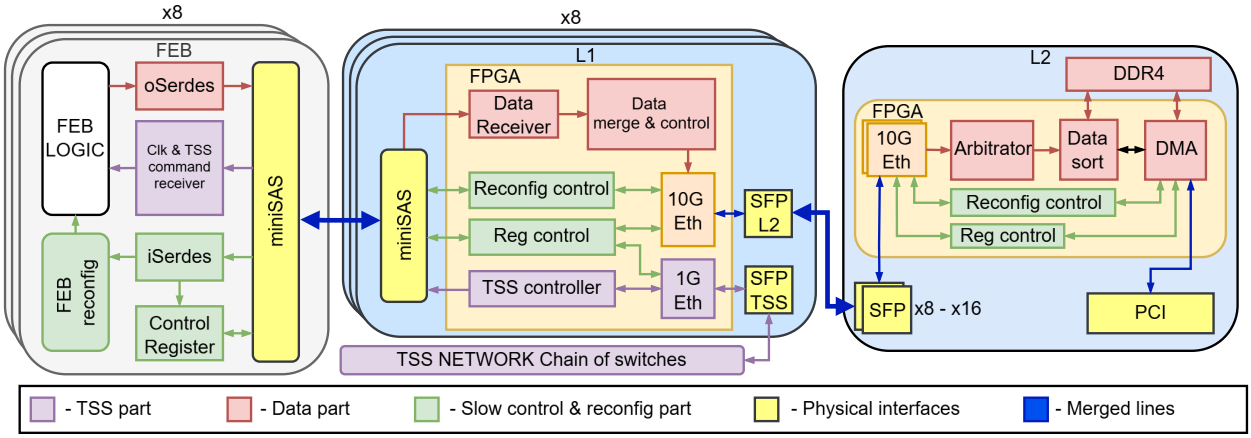

Figure 1: DAQ readout architecture.

The L2 concentrator is being developed on the commercially available ALINX Z19-P evaluation board with a Zynq UltraScale+ multiprocessor system-on-chip. The board is shown in Figure 2.

A critical stage in system integration is testing the connections between the L1 and L2 concentrators. This testing must verify the stability of data transmission under maximum load to prevent potential failures and data loss. Furthermore, it involves measuring the actual bandwidth of the optical links and comparing the results to theoretical values, ensuring they meet the experiment's requirements.

The test results will aid in identifying any shortcomings, optimizing overall system

Figure 2: Hardware platform (Z19-P) of the L2 concentrator.

performance, and ensuring reliable operation under high-load conditions during the experiment.

To facilitate remote control of system components, such as Front-End Boards (FEBs) and L1 concentrators, specialized modules are necessary for transmitting slow control commands from servers to end devices. These modules must be integrated into the overall DAQ control system, guaranteeing seamless interaction between servers and low-level devices.

The objective of this work is to establish a stable optical connection between the L1 and L2 concentrators and to enable slow control command transmission from the L2 concentrator to L1.

To achieve this objective, the following scope of work is proposed:

1) Develop a module for assessing optical link quality.

2) Evaluate the stability of the optical connection.

3) Design and validate control command transceiver modules.

4) Configure a test stand with L1 and L2 concentrators.

2 IBERT IP core for optical link quality testing

The ALINX Z19-P hardware platform features two types of transceivers: GTY and GTH. These energy-efficient transceivers, based on the UltraScale architecture, support line rates ranging from 500 Mb/s to 16.375 Gb/s for GTH and from 500 Mb/s to 30.7 Gb/s for GTY. These highly configurable transceivers are tightly integrated into the UltraScale programmable logic, as described in [2] and [3].

In the Z19-P, GTH and GTY transceivers are each responsible for data transmission/reception on separate FMC interfaces. To maximize channel aggregation for L1, both interfaces must be utilized, providing a total of 8 to 16 full-duplex data channels.

For L1-L2 communication, optical fiber links compliant with the IEEE 802.3ae standard [4] are employed. Therefore, the test design must support a configurable number of channels and cross-family transceiver testing (e.g., GTY-GTH).

The design was implemented using Xilinx's IBERT IP core [5], wich is a highly configurable component. Its graphical configuration interface is shown in Figure 3.

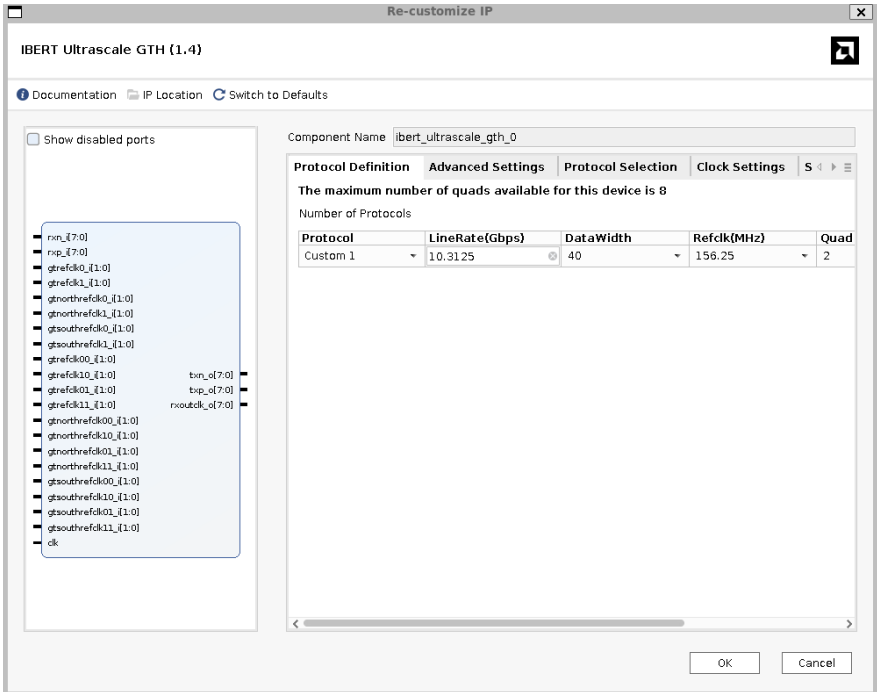

Figure 3: IBERT core configuration GUI

The core also provides real-time testing visualization, including eye diagram generation and dynamic SFP parameter adjustment during tests (see Figure 4).

To fully leverage these features, a custom module was developed, incorporating two IBERT cores (one for GTY, one for GTH transceivers).

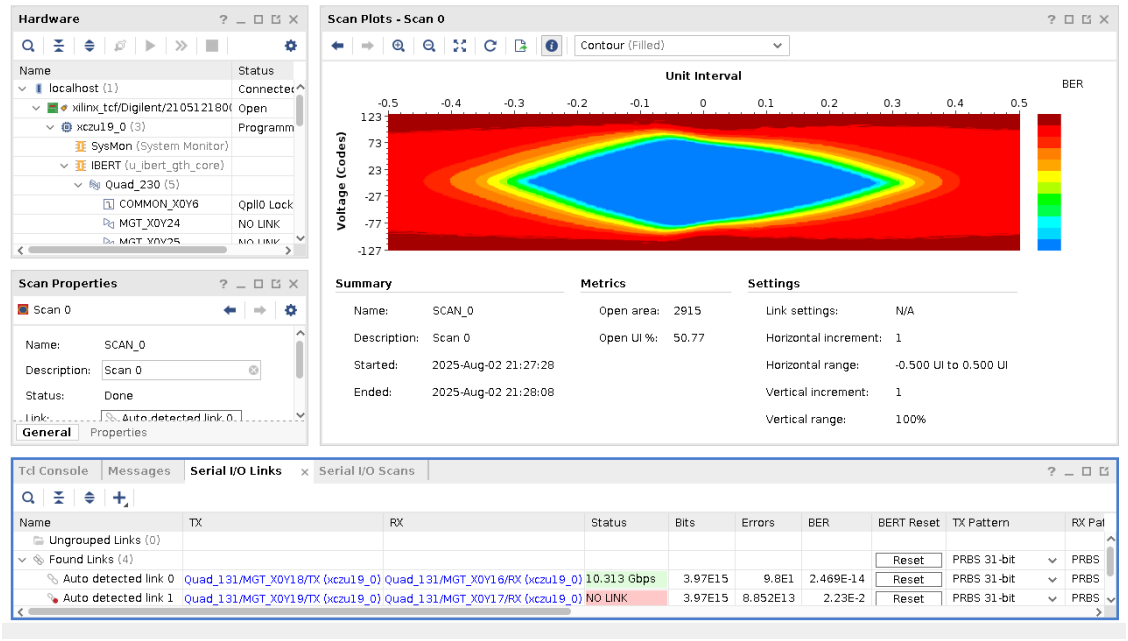

Figure 4: IBERT real-time monitoring interface

3 Optical link stability testing

For testing, we utilized multimode SFP modules (Ubiquiti uf-mm-10g) and a 3-meter multimode fiber cable. Connections were tested in configurations employing both transceivers of the same family and transceivers from different families (GTH-GTY).

According to the IEEE 802.3ae standard [4], the maximum permissible Bit Error Rate (BER) should not exceed 10^{-12}.

Figure 5 presents test results for the GTH-GTH configuration, demonstrating that the BER values remain within acceptable limits.

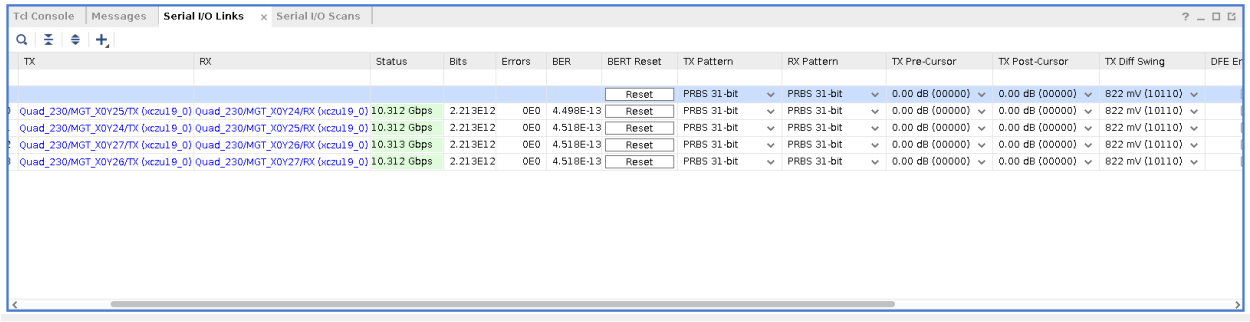

Figure 5: GTH-GTH configuration test results before transceiver tuning

However, this was not consistently observed across all configurations. Figures 6 and 7 display the results for the GTY-GTY and GTH-GTY configurations, respectively, revealing that some channels exhibit BER values exceeding the specified limits.

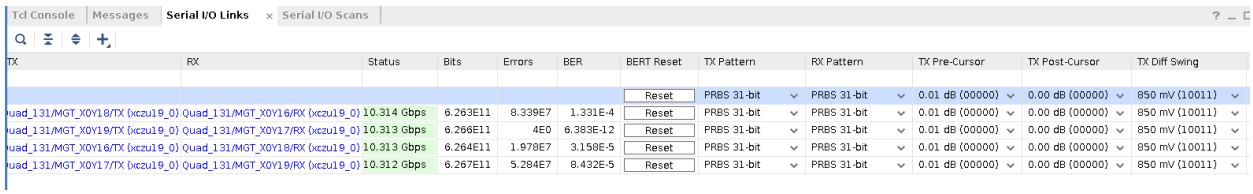

Figure 6: GTY-GTY configuration test results before transceiver tuning

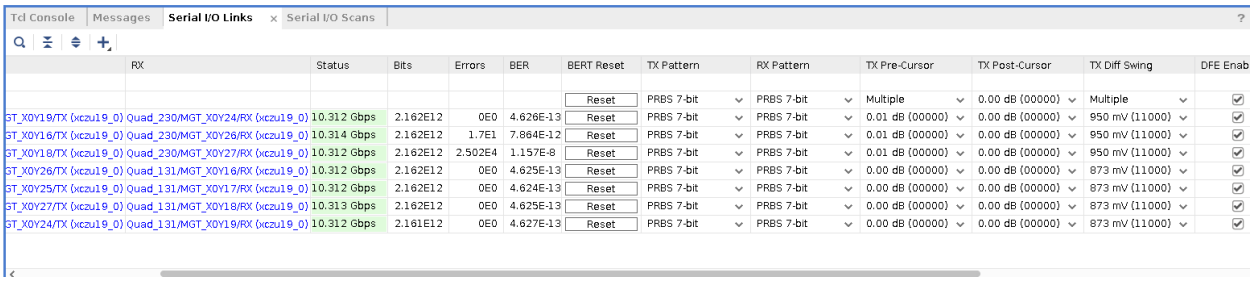

Figure 7: GTH-GTY configuration test results before transceiver tuning

To correct bit errors, we implemented pre-cursor and post-cursor settings, which serve to shape the signal pulse and maintain its integrity following optical transmission. The working principle of these settings is illustrated in Figure 8.

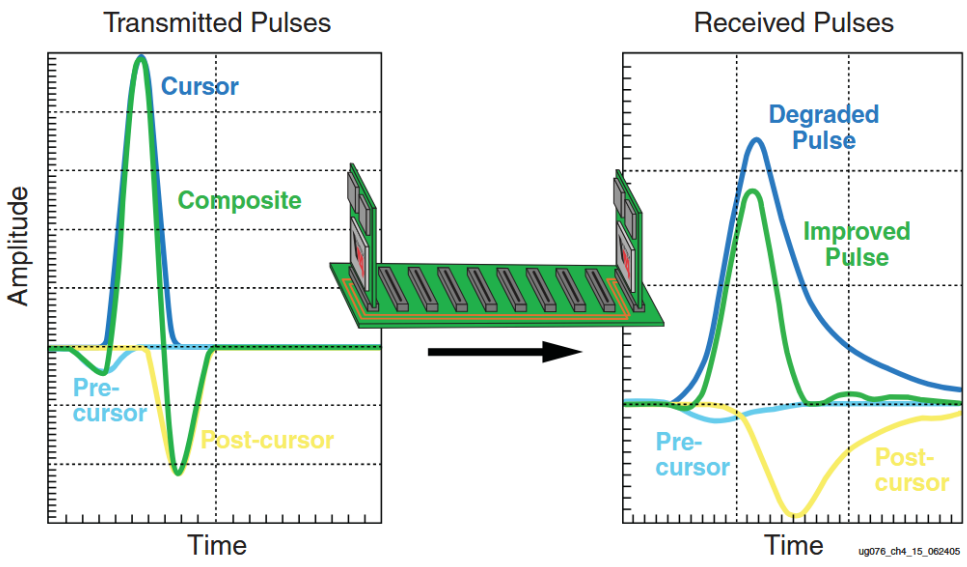

Figure 8: Operating principle of pre/post-cursor settings

After optimization of these parameters, we were able to achieve acceptable BER values, as shown in Figures 9 and 10. Thus, with transceiver tuning, we achieved optical link compliance with the IEEE 802.3ae standard.

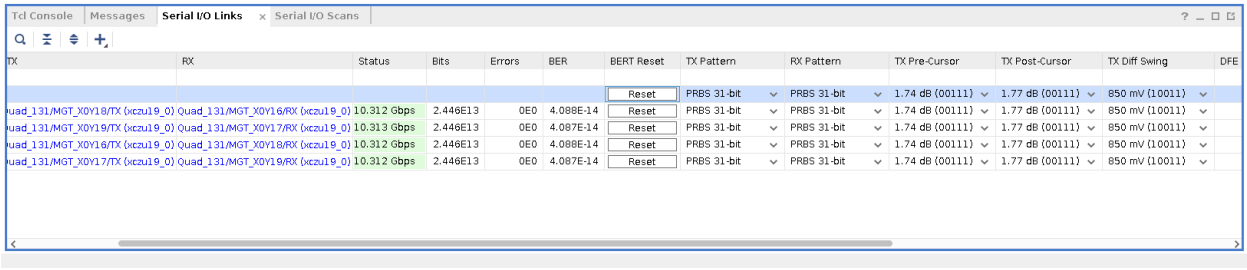

Figure 9: GTY-GTY configuration test results after transceiver tuning

TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing
						Reset	PRBS 31-bit	PRBS 31-bit	Multiple	Multiple	Multiple
Quad_131/MGT_X0Y19/TX (xczu19_0)	Quad_230/MGT_X0Y24/RX (xczu19_0)	10.313 Gbps	5.782E14	0E0	1.73E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.74 dB (00111)	1.77 dB (00111)	850 mV (10011)
Quad_131/MGT_X0Y17/TX (xczu19_0)	Quad_230/MGT_X0Y25/RX (xczu19_0)	10.312 Gbps	5.782E14	0E0	1.73E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.74 dB (00111)	1.77 dB (00111)	850 mV (10011)
Quad_131/MGT_X0Y16/TX (xczu19_0)	Quad_230/MGT_X0Y26/RX (xczu19_0)	10.312 Gbps	5.782E14	0E0	1.73E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.74 dB (00111)	1.77 dB (00111)	850 mV (10011)
Quad_131/MGT_X0Y18/TX (xczu19_0)	Quad_230/MGT_X0Y27/RX (xczu19_0)	10.312 Gbps	5.782E14	0E0	1.73E-15	Reset	PRBS 31-bit	PRBS 31-bit	1.74 dB (00111)	1.77 dB (00111)	850 mV (10011)
Quad_230/MGT_X0Y26/TX (xczu19_0)	Quad_131/MGT_X0Y16/RX (xczu19_0)	10.313 Gbps	5.782E14	0E0	1.73E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	707 mV (10010)
Quad_230/MGT_X0Y25/TX (xczu19_0)	Quad_131/MGT_X0Y17/RX (xczu19_0)	10.313 Gbps	5.782E14	0E0	1.73E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	707 mV (10010)
Quad_230/MGT_X0Y27/TX (xczu19_0)	Quad_131/MGT_X0Y18/RX (xczu19_0)	10.313 Gbps	5.782E14	0E0	1.73E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	707 mV (10010)
Quad_230/MGT_X0Y24/TX (xczu19_0)	Quad_131/MGT_X0Y19/RX (xczu19_0)	10.312 Gbps	5.782E14	0E0	1.73E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	707 mV (10010)

Figure 10: GTH-GTY configuration test results after transceiver tuning

4 Development and verification of eth2axi module

Synchronous and asynchronous (slow-control) commands are essential for the control and stable operation of the data acquisition system. Synchronous commands mark the start and the end of incoming data, while asynchronous commands carry system reset instructions. The latter type of command is transmitted to L1 via the L2 concentrator, necessitating the development of dedicated modules for the L2 and L1 concentrators to facilitate such transmission.

A slow control command is initiated from the readout computer and transmitted to the L2 board via the PCIe interface. It arrives at the module as an AXI-Lite transaction, which is then encapsulated into a Raw Ethernet packet, as detailed in [6]. This packet is transmitted to L1 through an optical link. The packet structures are illustrated in Figures 11 and 12.

To ensure compliance with the AXI-Lite specification, modules on the L1 side are required to generate responses to AXI-Lite transactions from the L2 board.

Figure 13 depicts the schematic of the "eth2axi" module, which is responsible for receiving Ethernet packets containing commands, decapsulating these packets, and generating appropriate responses.

The "eth2axi" module consists of several blocks, some of which were initially developed for the "axi2eth" module on the L2 concentrator side. The functionalities of these blocks are described below.

The "FIFO" module serves as a small buffer, introduced to delay the packet, allowing

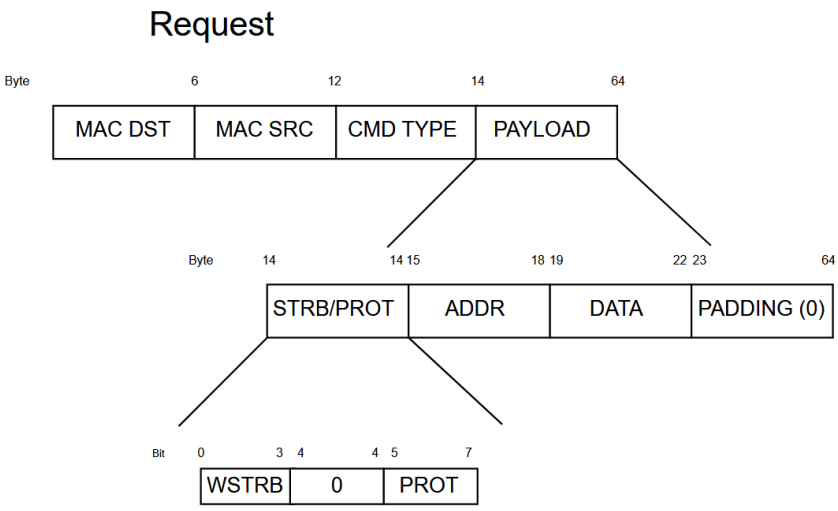

Figure 11: Structure of AXI-Lite request encapsulated in Raw Ethernet packet

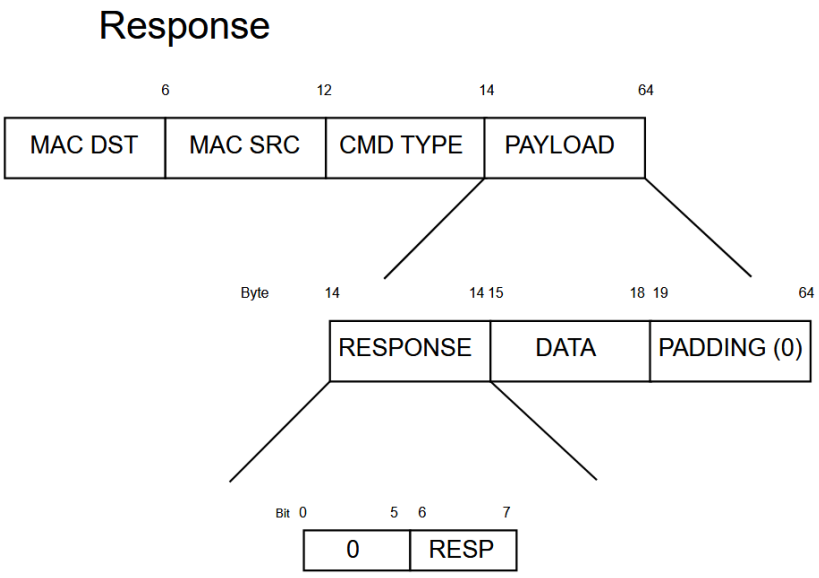

Figure 12: Structure of AXI-Lite response encapsulated in Raw Ethernet packet

for the retrieval of service information encoded in the last byte from upstream modules.

The "Receiver" module performs the decapsulation of the received Raw Ethernet packet, transforming it into an AXI-Lite transaction.

The "Buffer" modules function as buffers, temporarily holding AXI-Lite transactions.

The "Transmitter" module encapsulates the AXI-Lite transaction into a Raw Ethernet packet.

For module testing, a verification environment was developed in SystemVerilog. In addition, a Python script was created to emulate the "axi2eth" module, enabling the trans-

mission of AXI-Lite transactions directly from the computer's network interface card

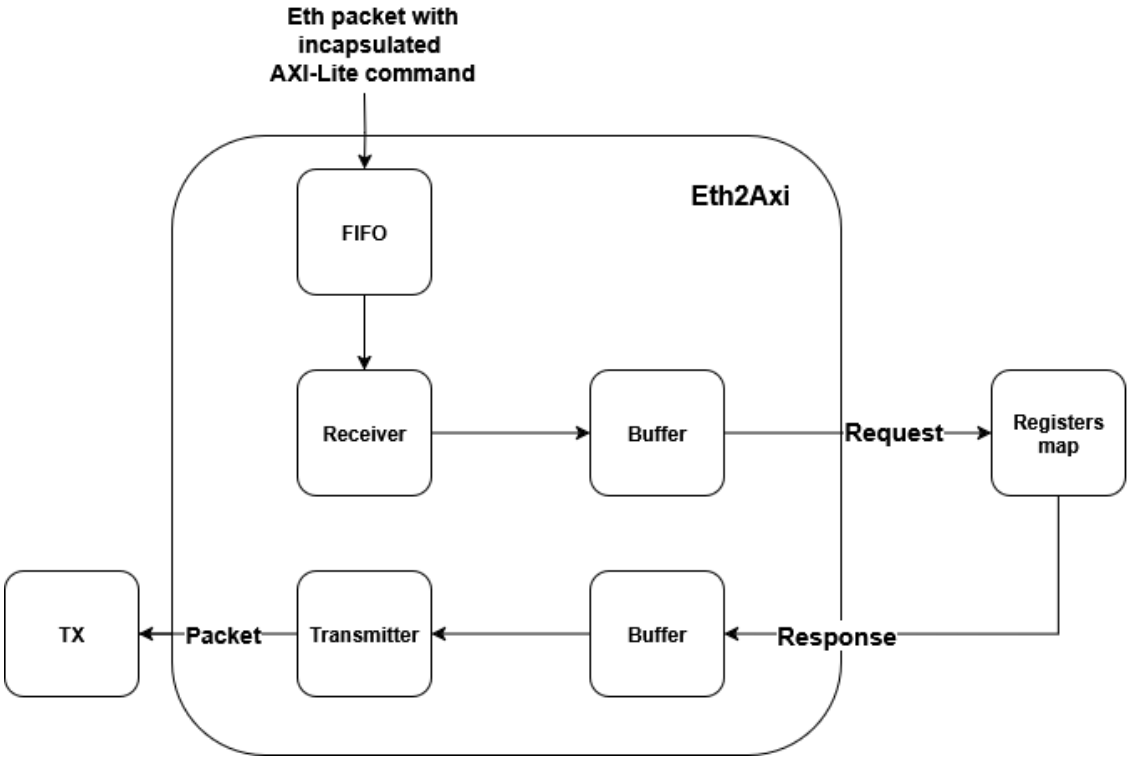

Figure 13: eth2axi module schematic

5 L2-L1 stand

To test the data readout chain under conditions as close to the experimental operation as possible, it is necessary to assemble a test stand that would incorporate all elements of the DAQ chain: front-end boards, L1 and L2 boards, and a readout computer. Assembly without them is a viable option that still provides extensive testing capabilities for the devices. The schematic of the L1-L2 test stand is shown in Figure 14

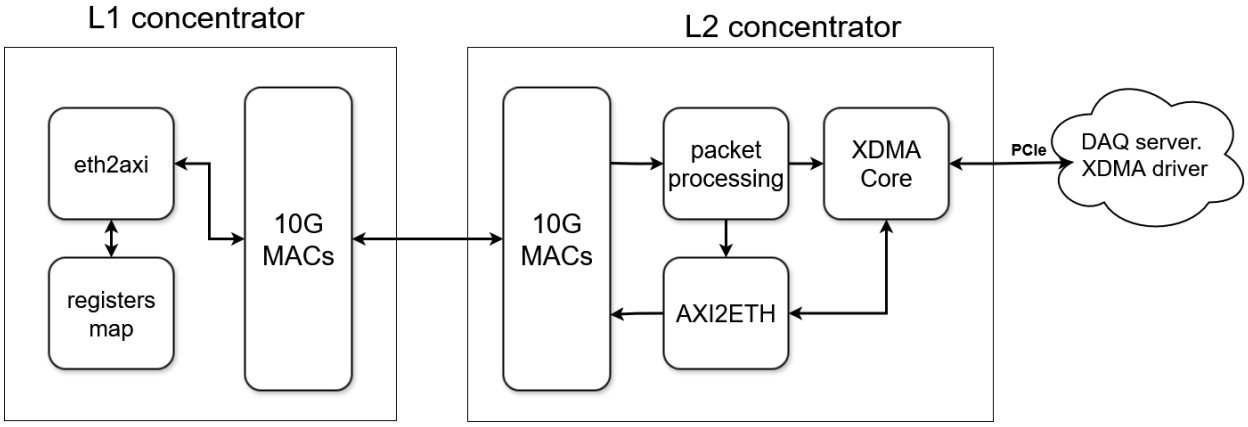

Figure 14: Schematic of the L1-L2 test stand

The L1 concentrator was configured with the following modules: 10G Ethernet, eth2axi, and registers map. This configuration enables the reception of Raw Ethernet packets containing encapsulated AXI-Lite transactions, forwards the transaction to the registers map, and generates a response to the received command.

On the L2 side, the firmware described in [6] was implemented. This firmware facilitates the transmission of commands from the computer to the L1 board via the axi2eth module. The hardware test stand is depicted in Figure 15.

The test results confirmed the transmission of commands generated on the computer to the L2 board and their arrival at the L1 concentrator. Upon receiving the transaction, L1 generates a response, which is then received by L2, validating the communication path.

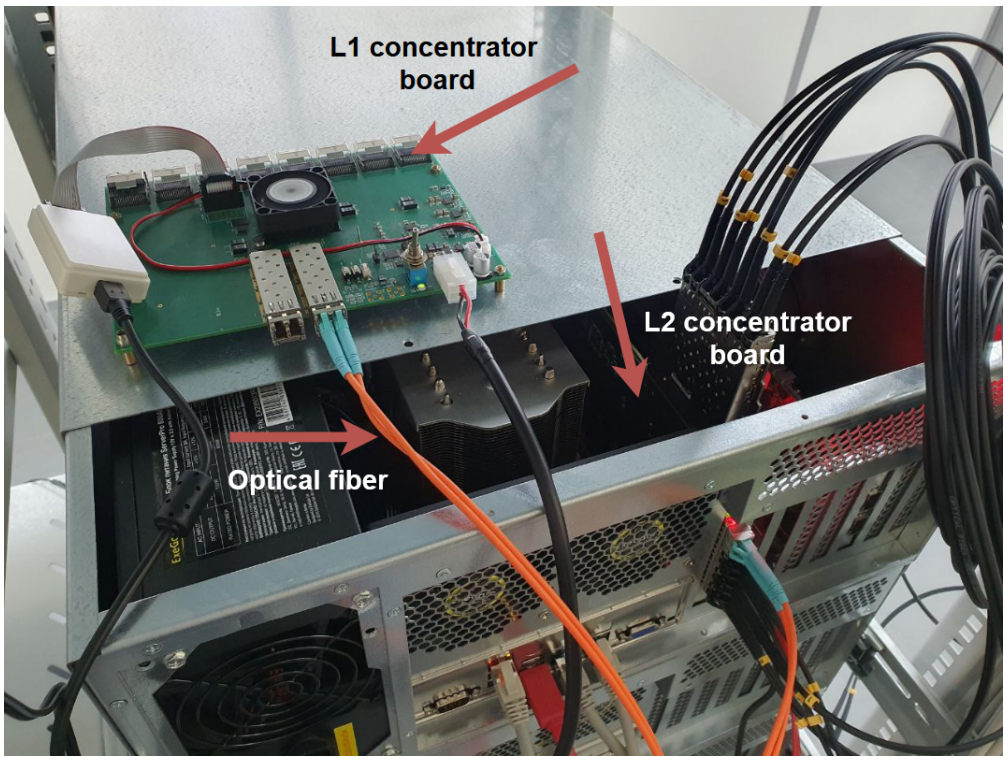

Figure 15: L1-L2 test stand

6 Conclusion

Optical link testing modules were developed and employed to verify and configure the transceivers, ensuring stable communication between the L1 and L2 concentrators.

To facilitate the reception of asynchronous commands, the eth2axi module was developed to decapsulate Raw Ethernet packets containing slow control commands originating from L2.

A test stand was constructed for L1-L2 concentrator integration, which will be utilized to evaluate interactions and data transmission between devices within the DAQ system.

The results obtained will be implemented during the integration of the L2 concentrator into the SPD experiment and in the development of slow control command handling modules for the L1 concentrator.

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