JOINT INSTITUTE FOR NUCLEAR RESEARCH
Dzhelepov Laboratory of Nuclear Problems

FINAL REPORT ON THE START PROGRAMME

Development of a hardware platform
for prototyping testbench electronics and data acquisition systems.

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Contents

Abstract

The Platform for prototyping electronics called SciPlatform is a flexible and affordable device that will be used during the development stages of electronics for different detector types.

The Platform consists of a main board containing the FPGA chip, front I/O 96 pin connector, UART and Ethernet interface IC's, and other supporting hardware. The front I/O connector accepts a range of different add-on boards with different hardware, which come with its own FPGA firmware, thus expanding the SciPlatform functionality.

Development of the Platform was chosen to be my project for this START session, and during it the FPGA main board was assembled and tested, an add-on discriminator card with 16 SMA inputs was designed and its PCB laid out, and FPGA firmware capable of receiving the discriminator signals, counting them, and sending the resulting data to the Readout PC through the UART interface was developed.

Additionally, an FPGA Mezzanine Card with 8 SFP+ transceiver ports was redesigned and manufactured.

1 Introduction

The goal of this START session was the development of the SciPlatform - an affordable and flexible device that will be used during the development stages of electronics for different detector types. Development included a range of different tasks, such as analog and digital circuit design, PCB design, and FPGA firmware development.

FPGA main board assembled and tested for operation. The FPGA firmware consisting of an impulse counter with AXI-Lite output and an AXI-to-UART interface was designed. A 16 channel discriminator add-on board circuit was designed and a PCB was laid out.

2 Sci-Platform

SciPlatform is a flexible and affordable platform for creating target electronics for testing detectors during the research and development phase. The main idea is to create a modular architecture that will consist of a main board with an FPGA chip and several add-on modules with matching firmware for the FPGA chip.

The add-on modules can perform a variety of different functions, such as LED drivers, discriminators, trigger modules, scalers, time-to-digital converters, delay modules, attenuation and amplification modules, etc.

Some of the possible uses for the Platform are: getting dark count graphs, photoelectron spectrums, etc. of silicon or tube type photomultipliers and similar tasks for other types of detectors.

The main board structure is shown in the block diagram in Figure 1. It includes a Cyclone 10 LP FPGA chip, an Ethernet PHY with an RJ45 jack, a UART to USB IC for control and data readout, and a 96 pin Front I/O connector for the add-on cards. The FPGA firmware can be stored and flashed after a power cycle using the onboard 16 Mbit EPCS IC.

The board is powered by a +12V power supply and the voltages necessary for the FPGA and add-on module operation, such as +6V, +3.3V, +2.5V, and 1.2V are generated by the power stages on the main board.

Additionally, the main board has SMD switches that can be used for addressing on an Ethernet network, 10 LED's for status signals, and a physical reset button.

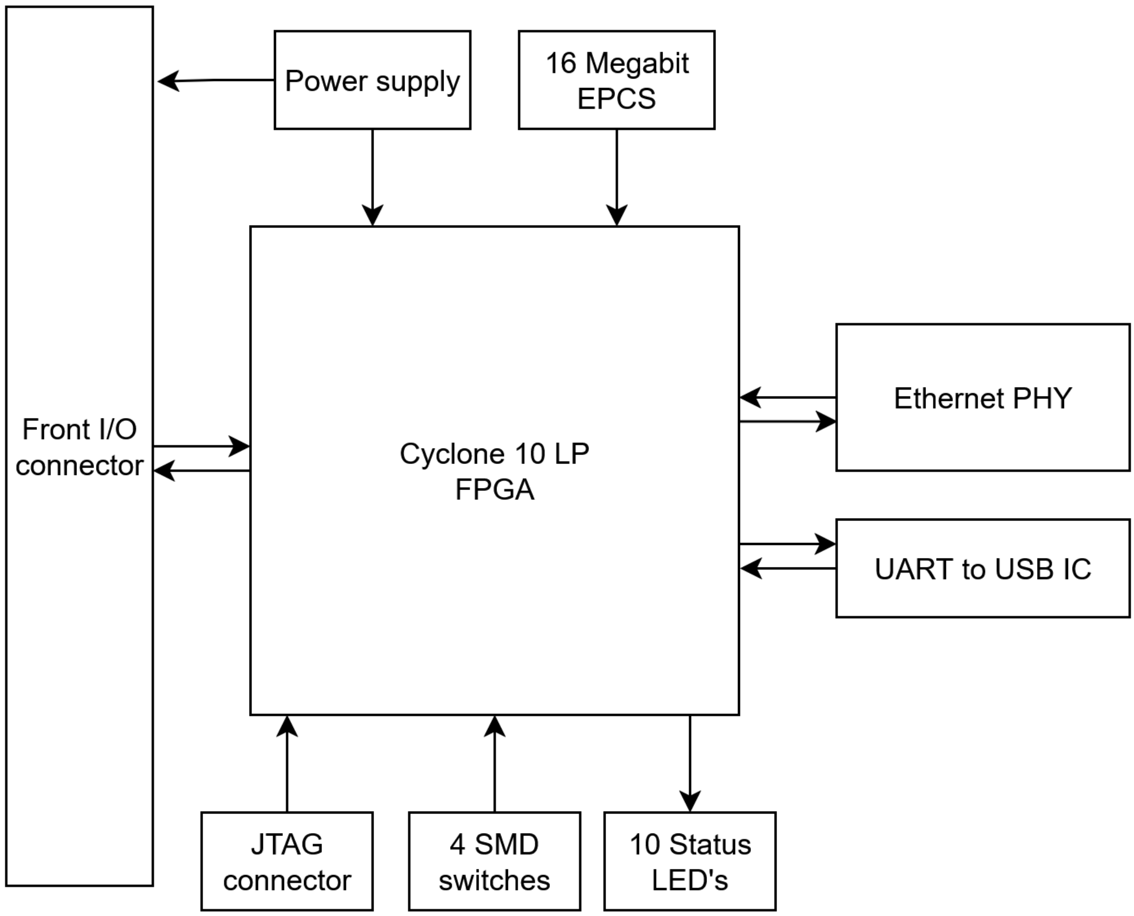

Figure 1: SciPlatform main board block diagram

The main board was assembled and tested for operation. It was successfully programmed through the JTAG interface with a base project which routed the input clock signal from a crystal generator on the PCB through a PLL to all the Front I/O connector outputs. A photo of the assembled board can be seen in Figure 6.

Discriminator add-on board that should accept analog signals and compare them to a reference voltage set by the user was designed. The resulting signals will be accepted and counted by the FPGA board when a trigger signal is present.

This board can be used for tasks mentioned earlier, such as gathering dark count data and photoelectron spectrum from silicon and tube style photomultipliers, and acquiring characteristic data for various other detector types.

The board consists of 16 AD8561 comparators and 2 AD5328 DAC's controlled over SPI protocol. It includes an LM317 based power supply providing +5V comparator power, an ADP3334 LDO voltage regulator forming the 2.5v pull up voltage for the input, 16 SMA input jacks, and a 96 pin connector to connect it to the main board. The board's functional block diagram can be seen in Figure 2.

DAC provides a reference signal for the first input of the comparator. The second input accepts the detector signal. The LDO provides a +2.5V bias to this input (half of the comparator input range), similar to a circuit found in [1]. This means that this design can discriminate between both positive and negative signals ranging from -2.5 to 2.5 volts.

The board was designed using a standard 4 layer 1/2 oz. copper stack up with a Signal-Power-Ground-Signal layout. 3D rendered images of the PCB can be seen in Figures 4 and 5.

The designed circuit was tested on a prototype board with the reference voltage and 2.5 volt shift provided by a laboratory power supply. The results are shown on the graph in Figure 3. Yellow - input square wave, Blue - input signal with the 2.5 v shift applied, Red - reference voltage which, when exceeded by the input, switches the comparator output to high, Green - resulting comparator output.

The circuit operation was confirmed, it was behaving as expected with a 10 MHz input signal frequency. The +2.5V operation point shift was applied successfully too.

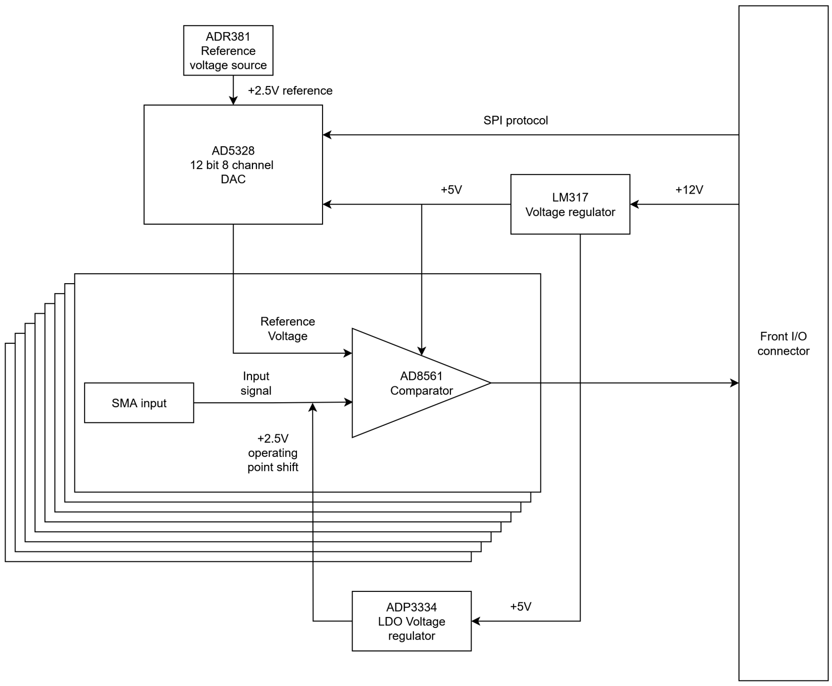

Figure 2: Discriminator PCB functional block diagram

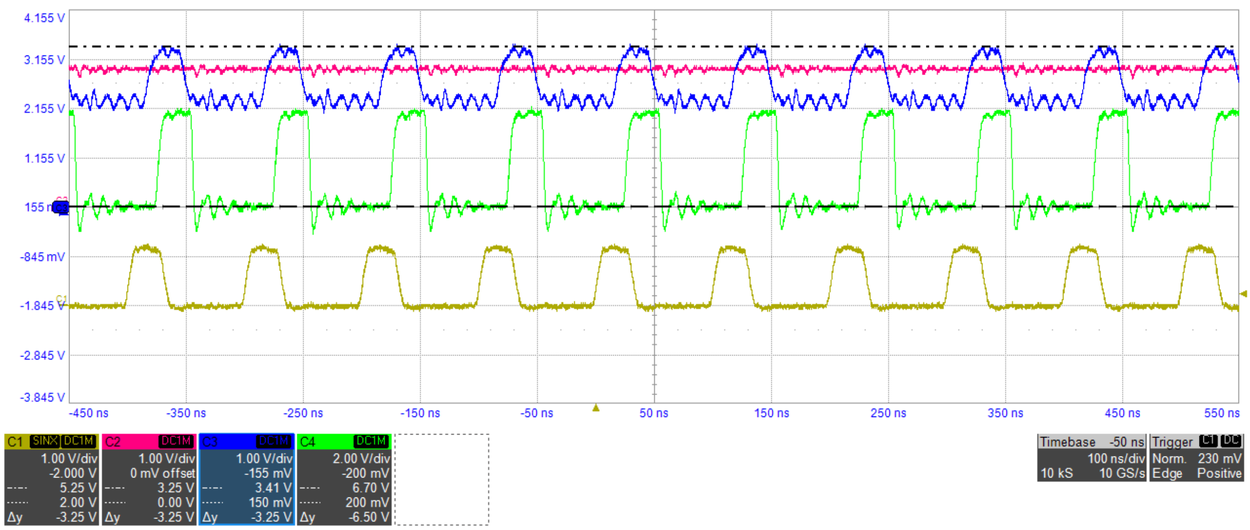

Figure 3: Captured signals from a prototype board

An FPGA firmware project was developed, including a counter which accepts signals from the comparator, detects the leading edge (one of the exercises in [2]), and counts the impulses, while an external trigger signal is present. After the trigger signal for the counter goes low, the data is saved and transferred to the AXI-to-UART module using AXI-Lite protocol, as described in [3]. This AXI-to-UART module then forms UART data stream and sends the data over to the Readout PC.

3 8 Channel SFP+ FMC board

Part of the data acquisition system of the SPD experiment at NICA is the L2 concentrator, described in the SPD Technical Design Report [4]. It gathers the data from up to 16 L1 concentrators over Ethernet, which accept the data from up to 16 front-end cards, thus one L2 concentrator collects the data from up to 256 channels, and transfers that data to the readout PC over PCI Express bus.

The L2 concentrator currently consists of a commercially available Z19-P Alinx FPGA carrier board with a Zynq Ultrascale+ FPGA chip and two Alinx FH1223 FMC to 4 SFP+ add-on cards. This board has two FPGA Mezzanine Card connectors, which have 8 GTH/GTY transceivers each, per Z19-P product page [5]. This means that this board is capable of accepting up to 16 SFP+ 10 Gbit transceivers, because both GTH and GTY transceivers are capable of working with 10G Ethernet, according to their respective documentation [6].

However, only 4 channel SFP+ FMC cards are commercially available (such as Alinx FH1223 [7]). Meaning that there is a need for an 8 channel FMC to SFP+ card, which would allow the L2 Concentrator to accept up to 16 L1 channels instead of the 8 possible now.

A matching PCB design was found in the CERN Open Hardware Repository [8]. However, it was not compatible with local manufacturing tolerances and had some minor errors.

This design was fixed and adapted for local manufacturing. The PCB was successfully manufactured. The photos of the PCB can be seen in Figures 7 and 8 of the Appendix.

4 Conclusion

Main board with the FPGA chip was assembled: +6, +2.5, +3.3 and +1.2V power stages, UART and Ethernet interface IC's, the FPGA chip and it's supporting components were installed. FPGA functionality was tested and the board confirmed working.

A 16 channel discriminator add-on board with 16 input channels and 2 DACs was designed. The circuit design was tested using a single channel prototype PCB.

First iteration of the FPGA firmware, consisting of a counter module with AXI-Lite interface and an AXI-to-UART module was created and tested for operation.

An 8 channel SFP+ FPGA Mezzanine Card add-on board design from CERN OHWR was modified, adopted for local manufacturing tolerances, and produced.

References

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[2] *Harris, Sarah L.* Digital Design and Computer Architecture / Sarah L. Harris, David Money Harris. — RISC-V edition. — Cambridge: Morgan Kaufmann, 2022. — P. 592.

[3] *ARM Holdings.* AMBA AXI and ACE Protocol Specification. — 2013. https://documentation-service.arm.com/static/5f915b62f86e16515cdc3b1c.

[4] *The SPD Collaboration.* Technical Design Report of the Spin Physics Detector at NICA. — 2024. https://arxiv.org/abs/2404.08317.

[5] *Alinx Electronic Limited.* Z19-P Product page. https://www.en.alinx.com/Product/SoC-Development-Boards/Zynq-UltraScale-plus-MPSoC/Z19-P.html.

[6] *Advanced Micro Devices.* AMD High Speed Serial Technologies. https://www.amd.com/en/products/adaptive-socs-and-fpgas/technologies/high-speed-serial.html.

[7] *Alinx Electronic Limited.* FH1223 Product page. https://www.en.alinx.com/Product/FMC-Cards/Communication/FH1223.html.

[8] *Filip Switakowski and Grzegorz Kasprowicz.* FMC SFP 4cha. — 2016. https://ohwr.org/projects/fmc-sfp-4cha/.

Appendix

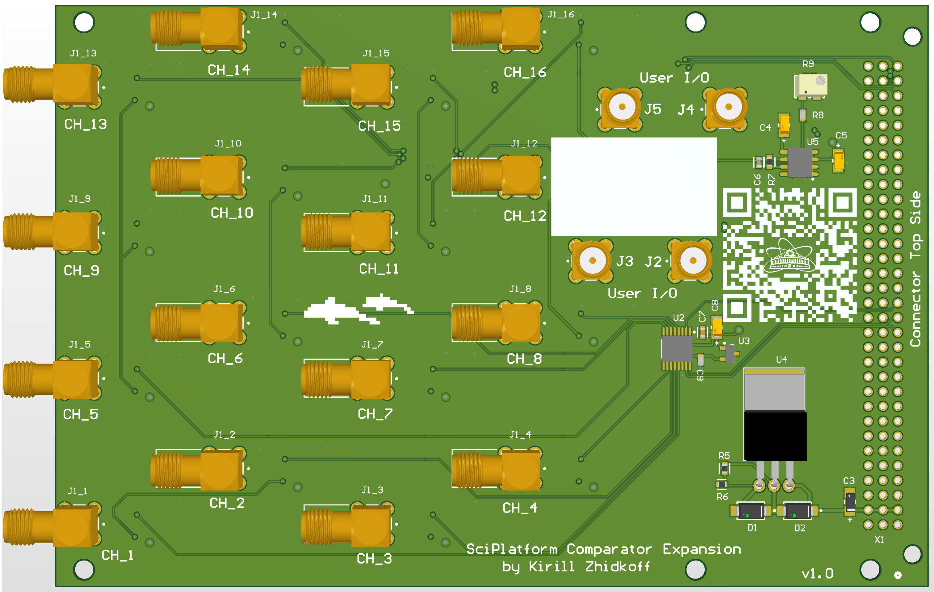

Figure 4: 16 channel discriminator PCB design (front side)

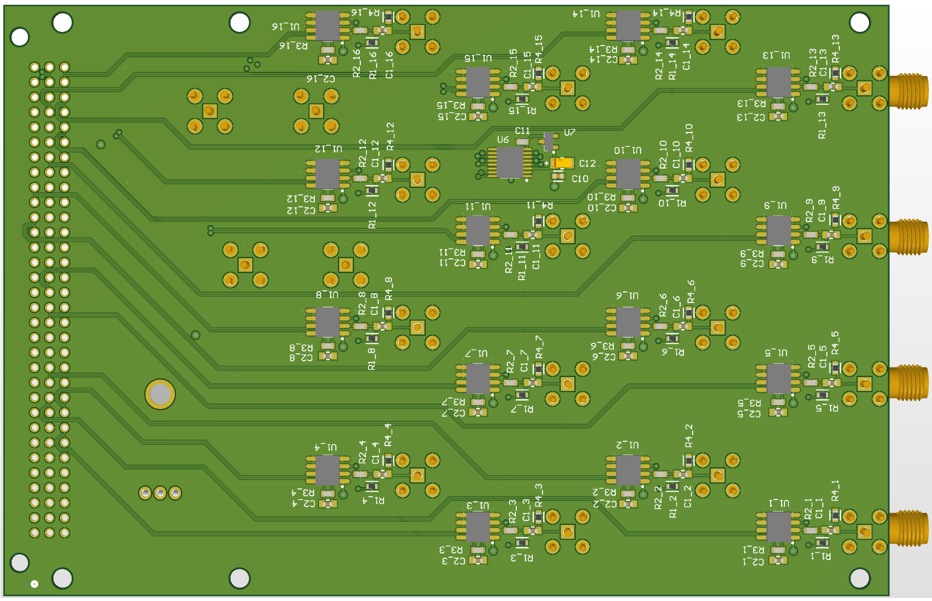

Figure 5: 16 channel discriminator PCB design (reverse side)

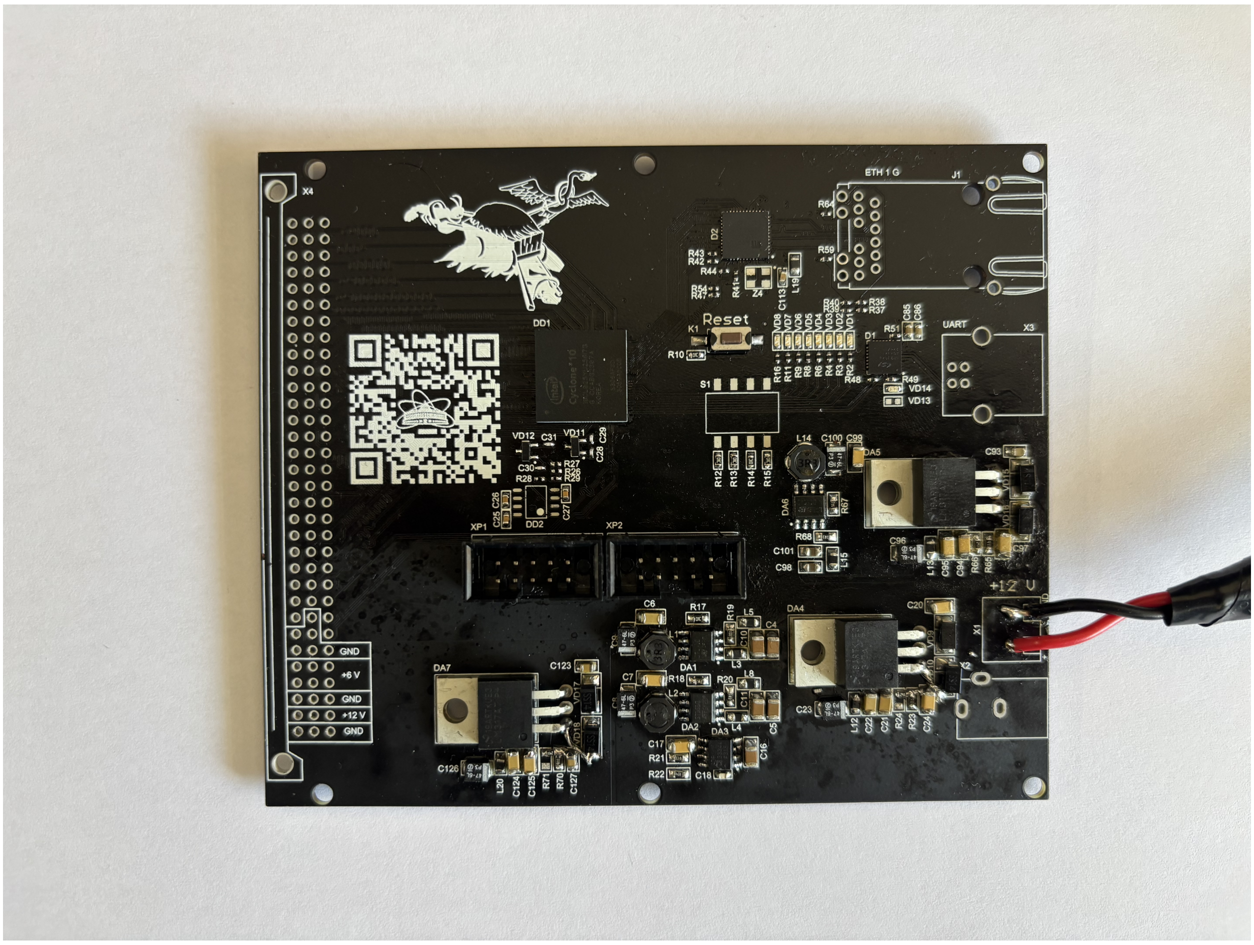

Figure 6: SciPlatform motherboard photo

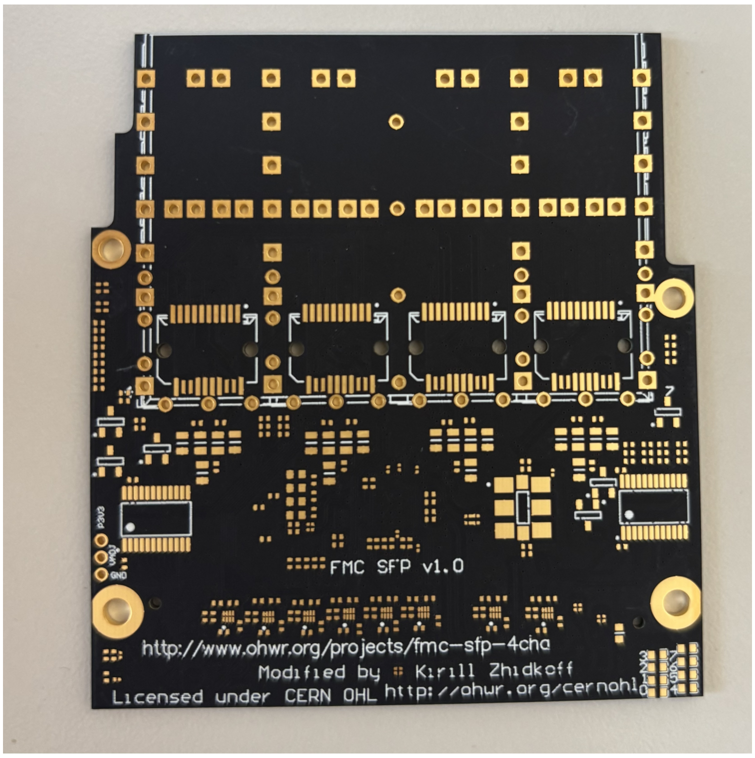

Figure 7: 8 channel SFP+ FMC PCB

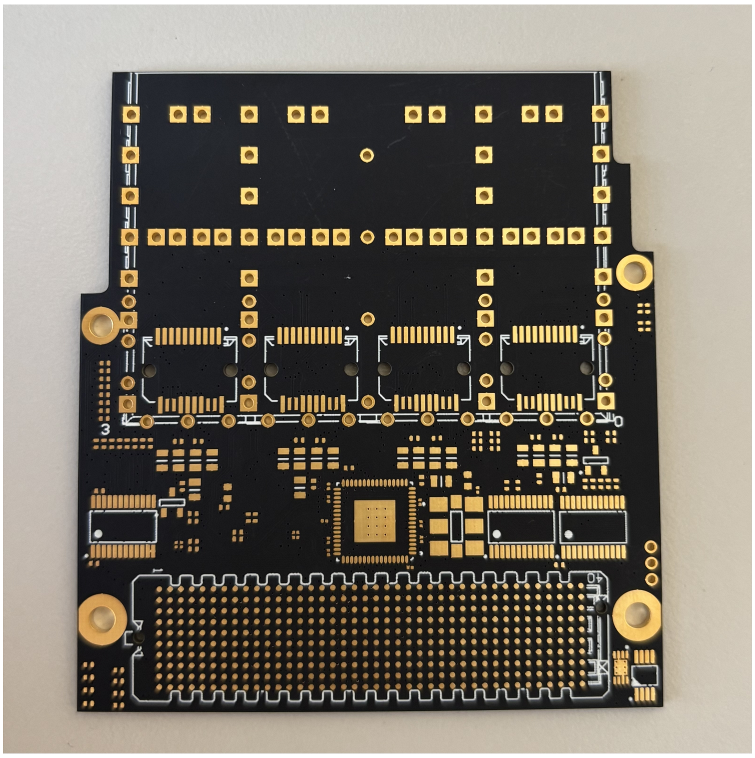

Figure 8: 8 channel SFP+ FMC PCB (reverse side)